Amendments to the Specification:

Please replace paragraph [0036] with the following amended paragraph:

[0036] In one embodiment of the invention, an optical lithography exposure system, generally referred to as a stepper, has a setting of members of a set of one or more optical parameters that control characteristics of exposures, the settings used to expose the phase shifting pattern and the complementary trim pattern used to produce an IC using phase shifting are unchanged, or otherwise kept substantially the same, between the exposures. This is applied for example when all, or substantially all portions, of a pattern are being defined using a phase shifting pattern on a mask, because there is minimal need to print small features using the trim pattern. Thus the trim pattern consists of features that have greater design latitude in exposure settings ~~that~~ than do the features formed using the phase shifting pattern, and can be exposed with key optical settings such as one or more members of a set of optical parameters including numerical aperture (N.A.), wavelength (λ) of light, coherency (such as measured by partial coherence σ), illumination configuration (single spot source, dipole source, quadrapole source, annular source), axis of illumination, and defocus, in various combinations.

Please replace paragraph [0039] with the following amended paragraph:

[0039] In other embodiments, the relevant layout comprises a layout where phase shifting is used to define at least one of:

- eighty percent (80%) of non-memory portions in one layer of material in the layout;
- eighty percent (80%) of a part of the floorplan in one layer of material;
- eighty percent (80%) of cells in a given area;
- ninety percent (90%) of a layer of material;
- ninety five percent (95%) of a layer of material;
- ninety nine percent (99%) of a layer of material;
- one hundred percent (100%) of a layer of material;

- one hundred percent (100%) of ~~a in~~ a functional unit of the chip (e.g. ALU) in one layer of material;
- one hundred percent (100%) of features in a layer of material that are in the critical path of the design;
- one hundred percent (100%) of features in a layer of material above or below certain dimensions, e.g. all features with a critical dimension 50 μm < CD < 100 μm;
- everything in a layer of material except those features that cannot be phase shifted due to phase conflicts that cannot be resolved;
- everything in a layer of material except test structures; and
- one hundred percent (100%) of all non-dummy features, e.g. features providing structural support for processing purposes, and non-electrically functional features in a layer of material.

Please replace paragraph [0040] with the following amended paragraph:

[0040] By maintaining a high coherency illumination setting (low partial coherence σ) for both the phase shifting and binary trim pattern on a mask, it is possible to more quickly, and accurately, produce ICs where all or substantially all of the pattern features are defined using phase shifting. In one embodiment, the percentages are determined based on the number of edges, or edge segments, within the pattern defined using phase shifting.

Please replace paragraph [0048] with the following amended paragraph:

[0048] FIG. 4 illustrates a single reticle having both [[a]] phase shifting and trim patterns. In this example, the reticle 400 includes a phase shifting pattern 402 and a trim pattern 404. The phase shifting pattern 402 shows a pattern "1" and the trim pattern 404 a pattern "2" for convenience of explanation of the wafer exposures described below.

Please replace paragraph [0051] with the following amended paragraph:

[0051] In one approach, the dosing will be maintained at equal levels for the phase shifting and trim ~~and binary~~ exposures. Turning to FIG. 5, a wafer 500 is shown after the first exposure. The wafer 500 has the alternating 1-2 pattern caused by the exposure of some regions to the phase shifting pattern and the exposure of other regions to the trim pattern 404. A second exposure, shown in FIG. 6, of the wafer 500 completes the process once the reticle and/or wafer has been repositioned within the stepper. FIG. 6 illustrates the pattern as 12 or 21 depending on the order of exposure for a region.

Please replace paragraph [0053] with the following amended paragraph:

[0053] FIG. 9 illustrates a single reticle having phase shifting pattern and two trim patterns. In this example, the reticle 900 includes a phase shifting pattern 902, a trim pattern 904 and a trim pattern 906. In this embodiment, the trim pattern 904 and the trim pattern 906 are designed to produce the same pattern. Accordingly, by triple exposing the wafer a 1:2 dosing ~~ration~~ ratio between the phase shifting pattern and the trim patterns can be accomplished. The results are depicted in FIGS. 10-12 showing a portion of the wafer after the first exposure 1000, after the second exposure 1100, and after the third exposure 1200, respectively.

Please replace paragraph [0055] with the following amended paragraph:

[0055] The present invention also provides a method for manufacturing an integrated circuit. ~~Method~~ The method includes forming a layer of resist on a wafer at a first process station. The resist is cured and prepared for exposure using a stepper or scanner. The wafer with a layer of resist is transported to the stepper. The stepper includes a radiation source, a mask and an optical path for exposing the wafer to radiation. The optical path is characterized by a set of optical parameters including one or more of a wavelength λ of illumination, numerical aperture NA, coherency, illumination configuration and defocus. In the stepper, the layer of resist is exposed to a

first dosing radiation to a phase shifting pattern in said mask using a first setting of the set of optical parameters. Next, the layer of resist is exposed to a second dose of radiation through the trim pattern in said mask using said first setting. Thus, the setting of the optical parameters is not changed between the exposures of the phase shift pattern and the trim pattern. As mentioned above, the mask may have more than one trim pattern and more than one phase shift pattern implemented thereon. In this case, the wafer may be subject to additional exposure steps, in which the settings of the optical parameters are not changed. The order of exposure of the phase shift pattern or patterns and trim pattern or patterns can be changed as suits a particular processing situation.

Please replace paragraph [0057] with the following amended paragraph:

[0057] After the exposure, the resist is developed using the techniques that are adapted for use with a particular resist involved. A pattern is left on the wafer which is used for a deposition and/or etching step to form ~~of~~ features of an integrated circuit. For example, the pattern may be used for etching an underlying layer of polysilicon to form interconnect, gate, capacitor, resistor and other circuit features on an integrated circuit.

Please replace paragraph [0059] with the following amended paragraph:

[0059] More specifically, current generation photoresist materials are chemically amplified so that exposure to light produces a very small number of acid molecules, that then continue to react. The passage of time and exposure to air may cause carbon dioxide, and other chemicals, to take up the acid and neutralize it. Using the single reticle approach, the photoresist should maintain its properties throughout both exposures and the timing between exposures can be shorter, allowing ~~and~~ more closely controlled ~~the effect~~ effects of exposure. Additionally, over time, the acid diffuses into the polymer.

Please replace paragraph [0064] with the following amended paragraph:

[0064] As used herein, the term optical lithography refers to processes that include the use of visible, ultraviolet, deep ultraviolet, extreme ultraviolet, x-ray, and other radiation sources for lithography purposes.